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System for transmitting LAN data frames through an ATM crossbar switch by using multiple request accessing

Technical field

The invention relates to the transmission of data frames between Local Area Networks (LAN) interconnected by a switch engine using the stack of multiple requests and relates in particular to a system for transmitting LAN data frames through an ATM crossbar switch by using multiple request accessing.

Background

Local Area Networks (LAN) such as Ethernet or token-ring networks, are generally interconnected through hubs. The hub is a system made of LAN adapters that communicate together through a switch card. This switch card can be either a

parallel bus or a passive switch card including a matrix for achieving the connection between selected inputs and outputs.

Today, the Asynchronous Transfer Mode (ATM) technology is growing very fast and most of the research developments are concentrated in high speed ATM networks instead of LANs. Very high speed ATM switches are now available and used for transferring data from two LANs connected to the switch. The use of the ATM technology for switching LAN frames requires to transform each LAN frame in splitting the frame into ATM frames by encapsulating them in the ATM Adaptation Layer (AAL) format. For this, the LAN frame coming from each line into the LAN adapter, with its destination address, is transformed onto AAL by a special module into ATM data packets before being transferred to the switch card for switching. Such a requirement results in two important drawbacks. Since the frame is converted into ATM cells, it is necessary to have a header in each cell containing protocol information such as the destination address. The same information is therefore repeated in each ATM cell, which represents many bytes that do not contain data and therefore there is an important waste of bandwidth. A further drawback is that the transformation of the LAN frame into ATM cells and the encapsulation in the AAL format require important hardware and software thereby resulting in a very important cost.

Furthermore, when a LAN adapter requests to transmit a LAN frame to another LAN adapter, it sends a request to the ATM switch wherein a scheduler determines whether it is possible to satisfy this request taking into account an algorithm which determines the best data connection to establish at each time. Accordingly, the grant signal to this request may be delayed during several time slots before being returned to the requesting LAN adapter while other requests are still awaiting in said LAN adapter.

Summary of the invention

Accordingly, the main object of the invention is to a system for exchanging data between a plurality of Local Area Networks (LAN) interconnected through an ATM crossbar switch wherein multiple requests from a LAN adapter may be sent to the switch without delaying these requests when a first request is awaiting for being granted.

The invention relates therefore to a data transmission system comprising a plurality of Local Area Networks LANs interconnected by a hub including a plurality of LAN adapters respectively connected to the LANs and an ATM crossbar switch interconnecting all LAN adapters wherein at least one of the LANs wants to transmit LAN data frames to several destination LANs, the LANs data frames being converted into concatenated slots of the same size and being transmitted through the ATM crossbar switch. The requesting LAN adapter comprises a control logic for transmitting a plurality of request signals (REQ) to the ATM crossbar switch, each of these requests being associated with a destination LAN, and the ATM crossbar switch comprises a scheduler for transmitting grant signals (GNT) respectively associated with the requests enabling the requesting LAN adapter to transmit LAN data frames to the destination LANs, the grant signals being transmitted in an order depending upon a predetermined algorithm controlling the scheduler regardless the order the requests are transmitted by the requesting LAN adapter.

Brief description of the drawings

The above and other objects, features and advantages of the invention will be better understood by reading the following more particular description of the invention in conjunction with the accompanying drawings wherein :

- Fig. 1 is a block-diagram of a data transmission system including four LANs interconnected by a hub according to the principles of the invention.
- Fig. 2 is a block-diagram of an ATM crossbar switch used within the hub illustrated in Fig. 2.
- Fig. 3 is a block diagram representing the main functions included in the scheduler of the ATM crossbar switch.
- Fig. 4A and 4B represent a time diagram showing the signals exchanged between the ATM crossbar switch illustrated in Fig. 2 and the LAN adapters according to the invention.
- Fig. 5 is a block-diagram of a LAN adapter within a data transmission system according to the invention.
- Fig. 6 is a block diagram representing the main functions included in the control logic of the ATM crossbar switch.
- Fig. 7 is a time diagram representing the main signals exchanged in a LAN adapter according to the invention.

Detailed description of the invention

The invention is implemented in an environment illustrated in Fig.1 wherein a plurality of Local Area Networks (LAN) 10, 12, 14, 16 are interconnected together by a hub 15 including an ATM crossbar switch 18 and the same plurality of LAN adapters. Each LAN is connected to switch 18 by means of a LAN adapter 20 for LAN 10, 22 for LAN 12, 24 for LAN 14 and 26 for LAN 16.

In reference to Fig. 2, an ATM crossbar switch used in the invention includes a data switch module 30, a scheduler 32, a plurality of LAN adapter connectors for connecting a same plurality of LANs to the ATM crossbar switch, only two LAN adapter connectors 34 and 36 being represented, and a clock generator 38 for supplying the clock and the synchronization to data switch module 30, to scheduler 32 and to the LAN adapter connectors.

Data switch module 30 includes a switching data block 40 which is generally a passive switching matrix between data input signals from the LAN adapters to the switching matrix and data output signals from the switching matrix to the LAN adapters. It also includes a control logic 42 which decodes the configuration signals received from scheduler 32 to determine the data path connections and establishes the data path connection based on the synchronization signal received from clock generator 38.

The scheduler 32 also includes an algorithm unit 46 which determines the best data connection to establish at each time. Such a determination is based on the selection of the request amongst all requests received from the LAN adapters which meets some predetermined criteria such as a priority order, the selection of unicast/multicast, the selection between reserved bandwidth data and non-reserved bandwidth data or any other criteria defined by the user.

A request signal is activated by a LAN adapter when it has a LAN frame to transmit to another LAN adapter through the ATM crossbar switch. Such a request signal is a serial encoded signal during the first two bytes of a time slot and includes 32 bits which are sampled by a signal the frequency of which is the data clock multiplied by 16. The first byte of the REQ signal includes the routing destination address on 16 bits, one bit per LAN adapter, a bit being set when the destination address corresponds to the associated LAN adapter. This encoding scheme allows either a point-to-point connection, a multicast connection or a broadcast connection. The second byte of the REQ signal contains the connection time on 16 bits, that is the number of time slots required to transmit the entire frame.

When receiving the grant signal from the control logic 44 of the scheduler, the LAN adapter transmits its frame. The GNT

signal generated by the control logic to is a serial encoded signal during the first two bytes of a time slot and includes 32 bits which are sampled by a signal the frequency of which is the data clock multiplied by 16. The first byte of the GNT signal includes the routing destination address on 16 bits, one bit per LAN adapter, a bit being set when the destination address corresponds to the associated LAN adapter. As for the REQ signal, the second byte of the GNT signal contains the connection time on 16 bits, that is the number of slots used for transmitting the frame.

The GNT signal includes information which are identical to the information contained in the REQ signal because the GNT signal is entirely de-correlated of the corresponding REQ signal. This means that any LAN adapter can send a plurality of requests and can receive a plurality of de-correlated signals.

As illustrated in more details in Fig. 3, the control logic 46 of scheduler 32 includes functional units enabling the requests from each adapter to be handled without delaying them because a previous request is awaiting for being processed. It includes principally a finite state machine FSM 50 which controls all steps performed from the reception of a request signal REQ to the transmission of a grant signal GNT. Note that the FSM 50 is timed by a clock control unit 52 which receives a clock signal and a synchro signal from the clock generator 38 (see Fig. 2).

When a REQ is received from a LAN adapted, it is deserialized by a serialized/deserializer SERDES 54, and transferred under control of FSM 50 to a memory interface 56. This REQ is stored into memory 58 to be worked out. Note that a plurality of REQs can be stored into memory 58 for each LAN adapter.

Periodically or as soon as a REQ is received from a LAN adapter, memory interface 56 provides algorithm 46 with the

REQs stored into memory 58 for each LAN adapter. Algorithm unit 46 selects a REQ among the plurality of REQs for each LAN adapter and provides REQ confirmation to FSM 50. Such a configuration is sent by FSM 50 to a configuration control block (CFG) 60 for being transmitted to the data switch module 30 (see Fig. 2) on the configuration data lines. At the same time, the selected REQs are transferred to serializer/deserializer 54 for being serialized and transmitted as grant signals GNT to the LAN adapters. For this, the frequency of clock signals issued from clock control unit 52 are multiplied by 16 in multiplier 53 and the resulting signals are used by SERDES 54 for generating the 32 bits of the GNT signal. Note that FSM 50 sends also information signals to memory interface 56 to indicate which REQs have been selected by algorithm unit 46 and have to be removed from memory 58.

The relationship between the signals at the interface between the ATM crossbar switch and LAN adapters are illustrated in Fig.4A and Fig. 4B. First, the data clock pulses are used to exchange the LAN frames between the adapters through the switch card. 53 clock pulses determine the time slot to exchange 53 data bytes corresponding to the ATM cell size. It must be noted that there is no requirement on the clock rate.

The SYNCHRO signal is a one pulse clock during the first data byte of each time slot. The REQ signal is active during the first two data bytes of a time slot. Then, the algorithm processing occurs during the following 51 bytes of the slot. Finally, a GNT signal delivered by the scheduler at the next time slot, is activated during the first two bytes of the following time slot. As previously mentioned the GNT signal corresponds to the selected configuration based on the Algorithm processing.

Thus, in Fig. 4A and 4B, a request X for transmitting n slots is received at the beginning of slot 1. At the same time a GNT signal is activated for a request C. Then, the request X is accepted by a GNT signal at the beginning of slot 2 during which data C are transmitted by the LAN adapter. At the beginning of the last slot (n+2) of the connection time during which the data X are transmitted by the LAN adapter, a REQ Y for two slots is accepted by a GNT signal. Then, the data corresponding to this GNT are transmitted by the LAN adapter during the two following slots, that is slots n+3 and N+4.

To summarize, at each synchronization pulse,the control logic 44 stores all REQ configurations from each LAN adapter at each time slot. Then, the algorithm 46 determines the best connection possible based on all stored REQ, sets the configuration data lines for the switch module 30 and activates the GNT signal to the selected LAN adapters. This new matrix switching state is latched up into switching matrix 40 on the falling edge of the GNT signal. This is done by control logic 42 of switching module 30.

In reference to Fig. 5, the hardware architecture of a LAN adapter is composed of a LAN logic 70 for processing the exchange of data with the LAN, a general bus 72 for transferring data bytes, a switch logic 74 for processing the exchange of data with the switch card, a system bus logic 76 for processing the transfer of data in the LAN adapter and an arbiter 58 for taking care of any bus contention for the requests which may come from LAN controller 74 or SCC 78 as well.

The LAN logic 70 comprises a LAN connector 80 allowing the connection of the LAN adapter to the LAN through a LAN attachment cable and carries the transmit data signal (TD) and the receive data signal (RD), an analog circuitry 82 for converting the TTL logic signals into analog and reciprocally

and for providing specified network characteristics such as impedance, capacitance, cross talk... LAN logic 70 also includes a LAN controller 84 which, when receiving a frame from LAN, performs the functions of :

- synchronizing its internal receive clock circuitry during the seven preamble bytes,
- detecting the LAN frame through the Start Frame Delimiter (SFD) byte,
- checking the data integrity of the frame by computing/comparing the four Frame Check Sequence (FCS) bytes,
- removing the protocol information such as preamble bytes, SFD byte and FCS bytes, and
- deserialising the remaining incoming bits to provide data bytes at the parallel interface with bus 72.

When transmitting data bytes from the parallel interface with bus 72 to the LAN, the LAN controller 84 performs the functions of :

- serializing the incoming parallel bytes,
- generating the protocol information bytes, and
- computing and sending the FCS bytes.

In the preferred embodiment, the LAN controller 84 is a master device with an internal DMA controlling the transfer of bytes on the parallel interface with bus 72.

The switch logic 74 includes a switch connector 86, a serial communication controller 88 for transmitting serial to the switch card through connector 86 and receiving data from the switch card through connector 86, a control logic 90 generating the request signal and synchronizing the timing between the switch card and the LAN adapter, and a clock multiplier 92 for providing control logic 90 with the transmit clock generating the request signal at a frequency being 16 times the frequency of the data clock.

Connector 86 allows the connection of the LAN adapter to the switch card through a back plane and carries the request signal (REQ), the grant signal (GNT), the transmit data signal (DATA OUT), the receive data signal (DATA IN), the data clock signal (DATA CLK) and the synchronization signal (SYNCHRO).

When transmitting data bytes from the parallel interface to the switch card, the serial communication controller 68 generates HDLC frames. It performs the functions of :

- generating an HDLC flag (one byte) to start a frame,
- serialising and sending the incoming parallel data bytes
- computing and sending the FCS (two bytes) after the data bytes, and
- generating an HDLC flag (one byte) to end the frame.

When receiving an HDLC frame from the switch card, the SCC (88) performs the hardware functions of :

- detecting the incoming frame through the flag,
- checking the data integrity of the frame by computing/comparing the Frame Check Sequence (FCS), and
- deserialising the incoming bits to provide data bytes at the parallel interface.

In the preferred embodiment, the SCC 88 is a master device with an internal DMA controlling the transfer of bytes on the parallel interface.

The system bus logic 76 includes a microcontroller 94 and a memory 96. Microcontroller 94 includes a processing unit, a ROS for storing the operational code, a RAM which operates like a cache memory and a programmable chip select for generating a memory chip select (CS1), a LAN controller chip select (CS2), a serial communication controller chip select (CS3) and a control logic chip select (CS4).

Memory 96 allows the LAN frame transfer between the LAN controller 84 and the serial communication controller. Such a memory is split in two independent areas, a LAN-to-switch area organized in a first plurality of 2K bytes buffers and a switch-to-LAN area organized in a second plurality of 2K bytes buffers.

It must be noted that the general bus 72 is made of a data bus, an address bus and control signals such as read, write, chip selects, interrupts, bus requests and bus acknowledges, bearing in mind that the width of both data bus and address bus is not critical.

The operation of the system according to the invention is as follows. Following a machine power-on or a reset, microcontroller 94 initializes the three main functions of the LAN adapter illustrated in Fig. 5, that is the memory 96, the LAN controller 84 and the SCC 88. The initialization of LAN controller 84 consists in setting up the receive DMA of the controller with the base address of the LAN-to-switch buffer # 1 in memory 96. The initialization of SCC 88 consists in setting up the receive DMA of the SCC with the base address of the switch-to-LAN buffer # 1 in memory 96.

Assuming that a frame is received from the network on the receive line TD of connector 60, this frame is converted into TTL logic by analog circuitry 82 and transferred to LAN controller 84. While the incoming bits are stored in an internal receive FIFO, the receive DMA of LAN controller 84 requests the use of general bus 72 to arbiter 78 by activating the HOLD signal. When the general bus 72 is free, arbiter 78 activates the HLDA signal. From now on, the receive DMA of LAN controller 84 transfers the bytes of the frame from the FIFO of the LAN controller wherein they are stored into the LAN-to-switch buffer # 1 in memory 96. When

the entire frame is stored in the memory, LAN controller 84 activates its interrupt signal INT1.

Wen receiving the interrupt signal INT1, microcontroller 94 stops its current task to execute a LAN interrupt routine by performing the actions of :

- reading the interrupt register of LAN controller 84 to determine the cause of the interruption,
- initializing the receive DMA of LAN controller 84 with the base address of the LAN-to-switch buffer # 2 in memory 76 (At this time a new frame coming from the network can be received),
- reading the frame byte count and the destination address, and
- jumping to a switch interface routine.

When running the switch interface routine, microcontroller 94 performs the actions of :

- determining the address of the destination LAN adapter using routing tables (it can be a unique address, a multicast address or a broadcast address),
- determining the Connection Time by dividing the frame count by 53,
- storing both the destination address and the connection time in a parallel-to-series register located in control logic 90.

The functions performed by control logic 90 are illustrated in Fig 6. When receiving the CS4 signal from the microcontroller 94, control logic 90 stores into a memory 102 by the intermediary of a data bus interface 100 the destination address and the connection time which are received from microcontroller 94 via bus 72. It must be noted that a signal CS4 is transmitted from microcontroller 94 to control logic 90 each time microcontrollet 94 is interrupted by the LAN controller 84 because a data frame is

received. Then, a finite state machine (FSM) 104 which controls all the operations of control logic 90, starts sending a REQ signal containing the destination address and the connection time through a switch interface control unit 106. Note that FSM 104 is timed by a clock control unit 110, this one providing also the clock of the REQ signal transmitted by switch interface control unit 106 from the data clock multiplied by 16.

When receiving a GNT signal, the switch interface control block 106 is activated for storing into the memory 102 the GNT contents and interrupting the finite state machine 104. The latter compares the destination address and the conection time of all requests stored in the memory 102 with the GNT contents. If the comparison is positive, FSM 104 programs the transmit DMA of the SCC 88 through the SCC interface 108 by sending to it the destination address and connection time through the data bus 72 using the data bus interface 100 and also activates the Clear-to-send line (CTS) to the SCC 68 through the SCC interface 108. The transmit DMA transfers the bytes from the LAN-to-switch buffer #1 of memory 96 into the switch card according to the received destination address and connection time of the GNT signal. These bytes are sent in an HDLC format to guarantee the data integrity through the backplane. When the LAN-to-switch #1 is empty, SCC 88 activates its interrupt line INT2. It must be noted that the HDLC format uses a flag when the end of the frame is reached even if the last slot is less then 53 bytes, and does not require the use of padding bits to complete a 53 bytes cells as in the ATM procedure.

Note that, it is the function of the Control Logic 90 to synchronize the timing of the different actions described above, such as outputting the destination address and the connection time on the request signal, getting the grant

signal and setting up the CTS signal, with the timing of the switch card. This timing is illustrated in Fig.7.

When receiving the interrupt signal INT2 from SCC 88, microcontroller 94 stops its current task to execute a SCC interrupt routine by performing the action of reading the interrupt register of SCC 88 to determine the cause of the interruption and releasing the LAN-to-switch buffer #1 in memory 96.

Reciprocally, when SCC 68 detects the reception of a frame from the switch card, it requests the use of the general bus 72 to arbiter 78 by activating its HOLD line and stores the incoming bits in an internal receive FIFO. When the general bus is free, arbiter 58 activates a HLDA line to SCC 88. From now on, the receive DMA of SCC 88 transfers the bytes of the frame from the FIFO of SCC 88 into the switch-to-LAN buffer #1 in memory 96. When the entire frame is stored in memory 96, SCC 88 activates its interrupt line INT2.

When receiving the interrupt signal INT2, microcontroller 74 stops its current task to execute the SCC interrupt routine by performing the action of :

- reading the interrupt register of SCC 88 to determine the cause of the interruption,
- initializing the receive DMA of SCC 88 with the base address of the switch-to-LAN buffer #2 of memory 96 (At this time a new frame coming from the switch card can be received),
- initializing the transmit DMA of LAN controller 84 with the base address of the switch-to-LAN buffer #1 of memory 96 and the byte count, and
- starting the transmit DMA of LAN controller 84.

Then, the transmit DMA of SCC 88 requests the use of general bus 72 to arbiter 78 by activating its HOLD line. When the

general bus is free, arbiter 78 activates the HLDA line to SCC 88. From now on, the transmit DMA of SCC 88 transfers the bytes of the frame from switch-to-LAN buffer #1 of memory 96 to the LAN. These bytes are transmitted serially through analog circuitry 82 onto the transmit line TD of connector 80. When the entire frame is sent out, LAN Controller 84 activates the interrupt line INT1 to microcontroller 94.

When receiving the interrupt signal INT1, microcontroller 94 stops its current task to execute the LAN interrupt routine by performing the actions of reading the interrupt register of LAN Controller 84 to determine the cause of the interruption and releasing the switch-to-LAN buffer #1.

CLAIMS

1. Data transmission system comprising a plurality of Local Area Networks LANs (10,12,14,16) interconnected by a hub (15) including a plurality of LAN adapters (20, 22, 24, 26) respectively connected to said LANs and an ATM crossbar switch (18) interconnecting all LAN adapters wherein at least one of said LANs wants to transmit LAN data frames to several destination LANs, said LANs data frames being converted into concatenated slots of the same size and being transmitted through said ATM crossbar switch;

said system being characterized in that said requesting LAN adapter comprises a control logic (90) for transmitting a plurality of request signals (REQ) to said ATM crossbar switch, each of said requests being associated with a destination LAN, and said ATM crossbar switch comprises a scheduler (32) for transmitting grant signals (GNT) respectively associated with said requests enabling said requesting LAN adapter to transmit LAN data frames to said destination LANs, said grant signals being transmitted in an order depending upon a predetermined algorithm (46) controlling said scheduler regardless the order the requests are transmitted by said requesting LAN adapter.

2. Data transmission system according to claim 1, wherein said requesting LAN adapter (20, 22, 24, 26) comprises a serial communication controller (88) including means for converting said LAN data frame received from said LAN into serial data having the form of concatenated slots of the ATM cell size in the HDLC format before transmitting said serial data to

said ATM crossbar switch (18) and means for converting serial data having the form of concatenated ATM cells received from said ATM crossbar switch into a LAN data frame before transmitting said LAN data frame to said LAN.

3. Data transmission system according to claim 2, wherein said request signals (REQ) are serial encoded signals of 32 bits and wherein said LAN adapter (20, 22, 24, 26) further includes a clock multiplier (92) for multiplying by 16 the data clock of the system and providing said control logic (90) with timing pulses used to transmit 32 bits of said request signals.

4. Data transmission according to claim 3, wherein said grant signals (GNT) are serial encoded signals of 32 bits which are sampled by a signal the frequency of which is the data clock of the system multiplied by 16.

5. Data transmission system according to claim 4, wherein both said request (REQ) and grant (GNT) signals include each a first data byte of 16 bits defining the destination address of said LAN data frames to be transmitted and a second data byte of 16 bits carrying the connection time defined by the number of slots to be transmitted.

6. Data transmission system according to claim 5 wherein said first data byte defining the destination address contains one bit for each LAN adapter, a bit being set when the destination address corresponds to the associated LAN adapter, allowing a point-to-point connection, a multicast connection or a broadcast connection.

7. Data transmission system according to any one of claims 2 to 6, wherein said serial communication controller (88) includes means for generating HDLC frames in response to said LAN data frames received from the LAN connected to said

LAN adapter before transmitting said HDLC frames to said ATM crossbar switch (18).

8. Data transmission system according to claim 7, wherein said generating means in said serial communication controller (68) includes means for generating an HDLC flag to start a frame, means for serializing the incoming parallel data bytes, means for computing the FCS after the data bytes and means for generating an HDLC flag to end the frame.

9. Data transmission system according to any one of claims 2 to 8, wherein said serial communication controller (88) includes means for converting HDLC frames received from said ATM crossbar switch (18) into LAN data frames to be transmitted to said another LAN.

10. Data transmission system according to claim 9 wherein said converting means in said serial communication controller (88) includes means for detecting a starting HDLC frame in the incoming HDLC frame, means for checking the data integrity of the frame by computing the FCS, and means for deserializing the data bits of the frame to provide the data bytes of said LAN data frame.

11. Data transmission system according to any one of claims 1 to 10, wherein said LAN adapter further comprises a memory (96) split into two independent areas, a first LAN-to-switch area organized in a first plurality of buffers for storing said LAN data frames received from the LAN connected to said LAN adapter and to be transmitted to another LAN, and a second switch-to-LAN area organized in a second plurality of buffers for storing said LAN data frames received from another LAN and to be transmitted to the LAN connected to said LAN adapter.

12. Data transmission system according to any one of claims 1 to 11, wherein said LAN adapter further comprises a LAN controller (84) for converting said LAN data frame received in serial form from the LAN connected to said LAN adapter into parallel data bytes and reciprocally.

13. Data transmission system according to claim 12, wherein said LAN controller (84) comprises means for synchronizing its clock during the preamble bytes when receiving said LAN data frame, means for detecting the incoming frame through the delimiter byte of said frame, means for checking the data integrity of said frame by computing the FCS bytes, means for removing the protocol information of said frame, and means for deserializing the remaining incoming bits of said frames to provide parallel data bytes.

14. Data transmission system according to claim 12, wherein said LAN controller (84) further includes means for serializing the incoming data bytes received from said serial communication controller (88), means for generating the protocol information bytes to be included in said LAN data frame, and means for computing the FCS of said frame before transmitting said frame to the LAN connected to said LAN adapter.

15. Data transmission system according to claim 12, 13 or 14, further comprising an arbiter (78) for taking care of the contention between requests to send from said LAN controller (84) and requests to send from said serial communication controller (88).

16. Data transmission system according to any one of claims 1 to 15, wherein said scheduler (32) comprises a control logic means (44) and an algorithm means (46), said control logic means including a memory (58) for storing said request (REQ) signals received from said requesting LAN adapter and said

algorithm means determining which is the request to be granted each time a new request signal is received, said request to be granted being used as a grant (GNT) signal being transmitted to said requesting LAN adapter.

System for transmitting LAN data frames through an ATM crossbar switch by using multiple request accessing

Abstract

Data transmission system comprising a plurality of Local Area Networks LANs (10,12,14,16) interconnected by a hub (15) including a plurality of LAN adapters (20, 22, 24, 26) respectively connected to the LANs and an ATM crossbar switch (18) interconnecting all LAN adapters wherein at least one LAN wants to transmit LAN data frames to several destination LANs, the LANs data frames being converted into concatenated slots of the same size and being transmitted through the ATM crossbar switch. The requesting LAN adapter comprises a control logic for transmitting a plurality of request signals (REQ) to the ATM crossbar switch, each of them being associated with a destination LAN, and the ATM crossbar switch comprises a scheduler for transmitting grant signals (GNT) respectively associated with the requests enabling the requesting LAN adapter to transmit LAN data frames to the destination LANs, the grant signals being transmitted in an order depending upon a predetermined algorithm controlling the scheduler regardless the order the requests are transmitted by the requesting LAN adapter.

FIG. 1

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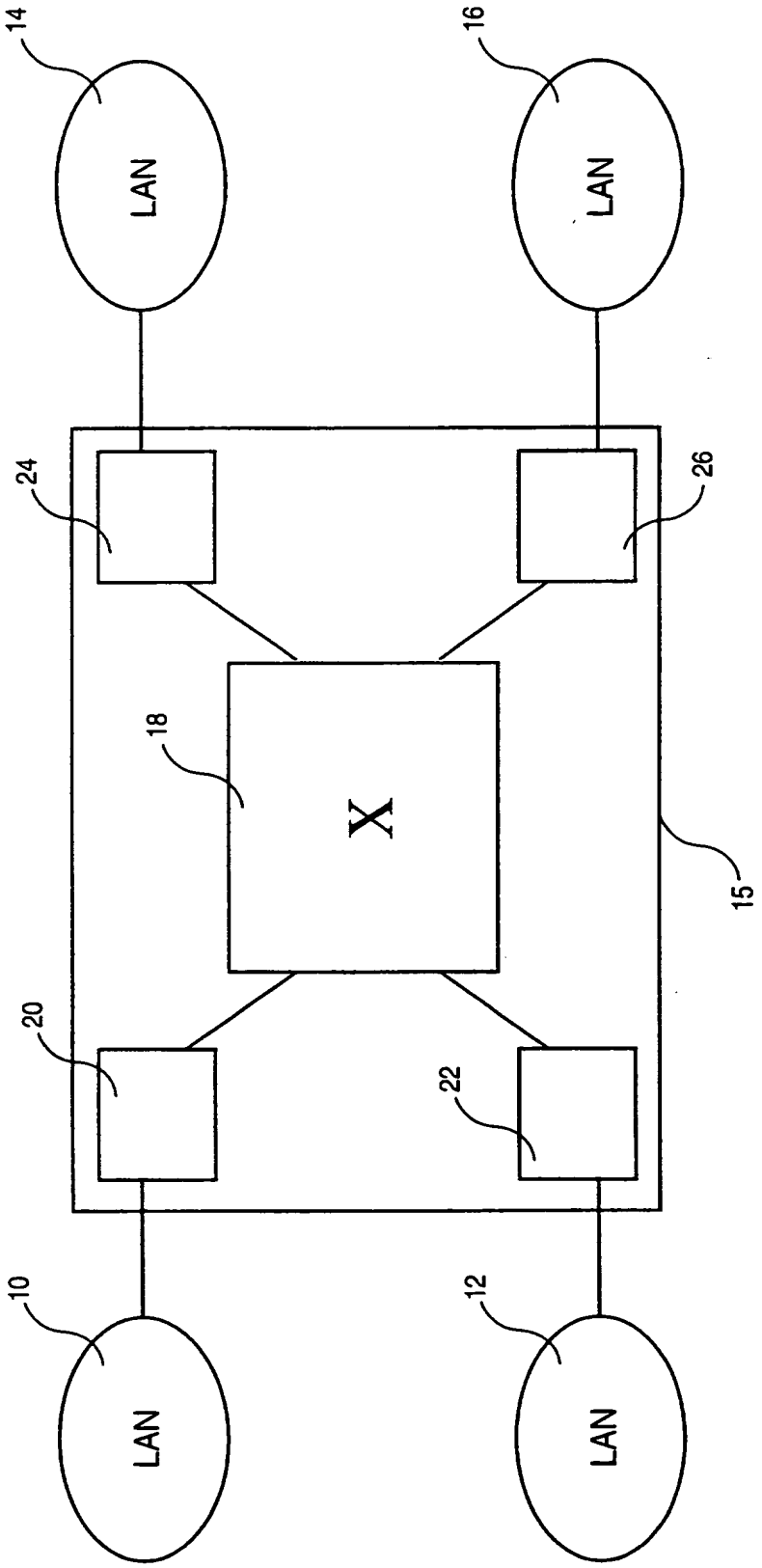

FIG. 1

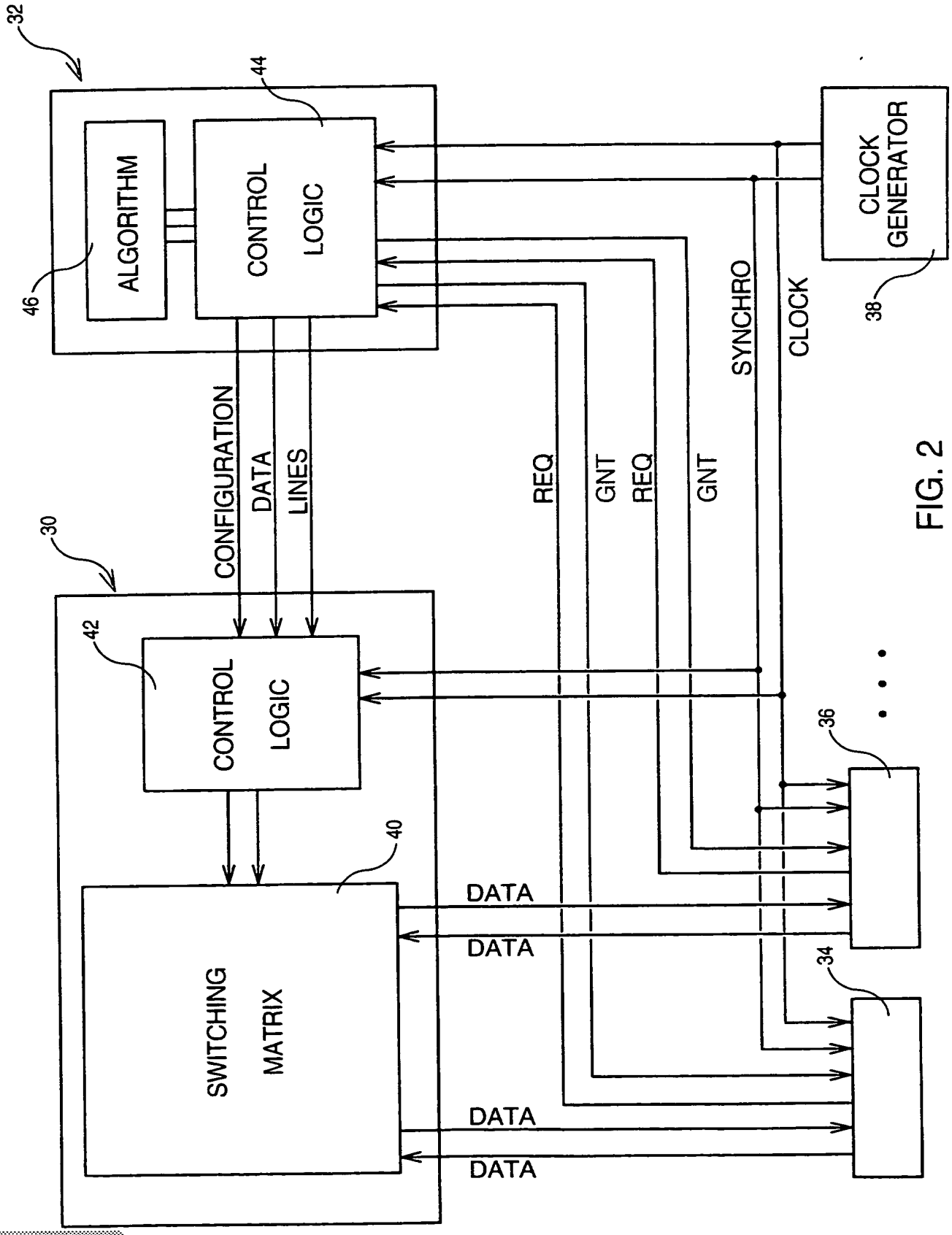
32
44
ALGORITHM
CONTROL LOGIC
46
CLOCK GENERATOR
38
SYNCHRO
CLOCK
CONFIGURATION DATA LINES
REQ
GNT
REQ
GNT
30
42
CONTROL LOGIC
36
40
SWITCHING MATRIX
DATA
DATA
34
DATA
DATA

FIG. 2

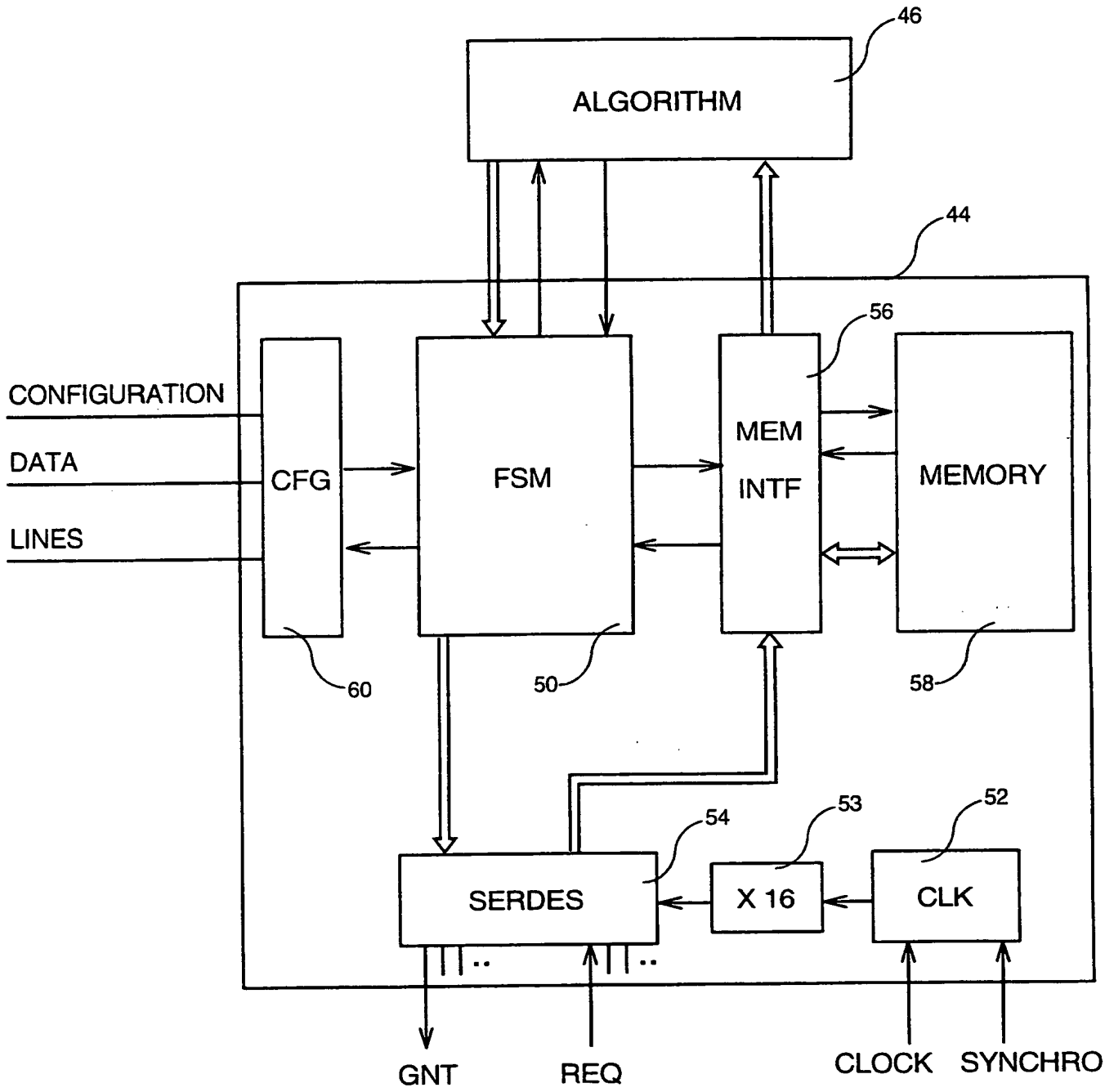
46
ALGORITHM
44
56
CONFIGURATION
DATA
LINES
CFG
FSM
MEM
INTF
MEMORY
60
50
58
54
53
52
SERDES
X 16
CLK
GNT
REQ
CLOCK
SYNCHRO

FIG. 3

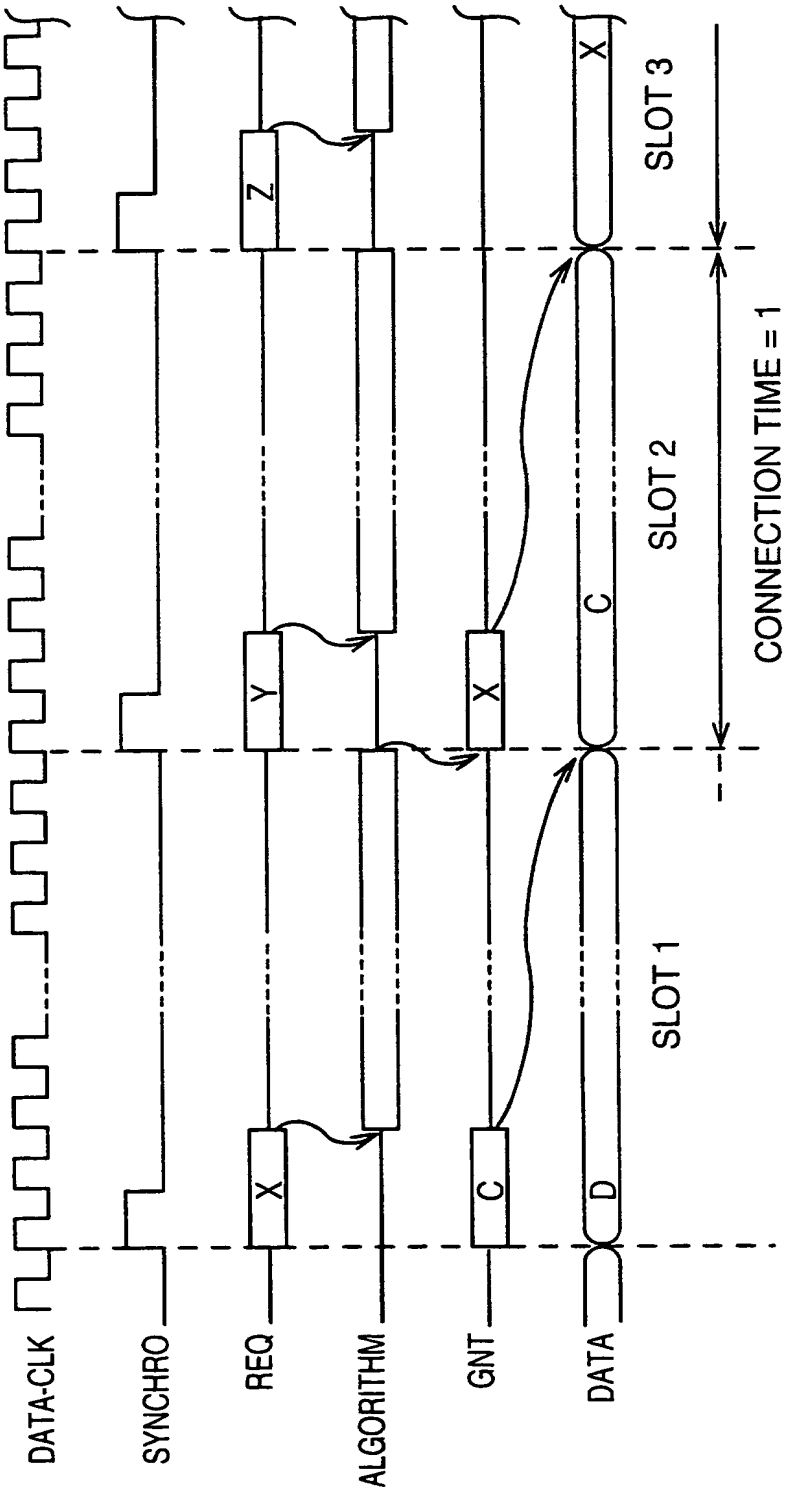
DATA-CLK
SYNCHRO
REQ
ALGORITHM
GNT
DATA
X
Z
Y
X
C
X
C
D
SLOT 1
SLOT 2
SLOT 3
CONNECTION TIME = 1

FIG. 4A

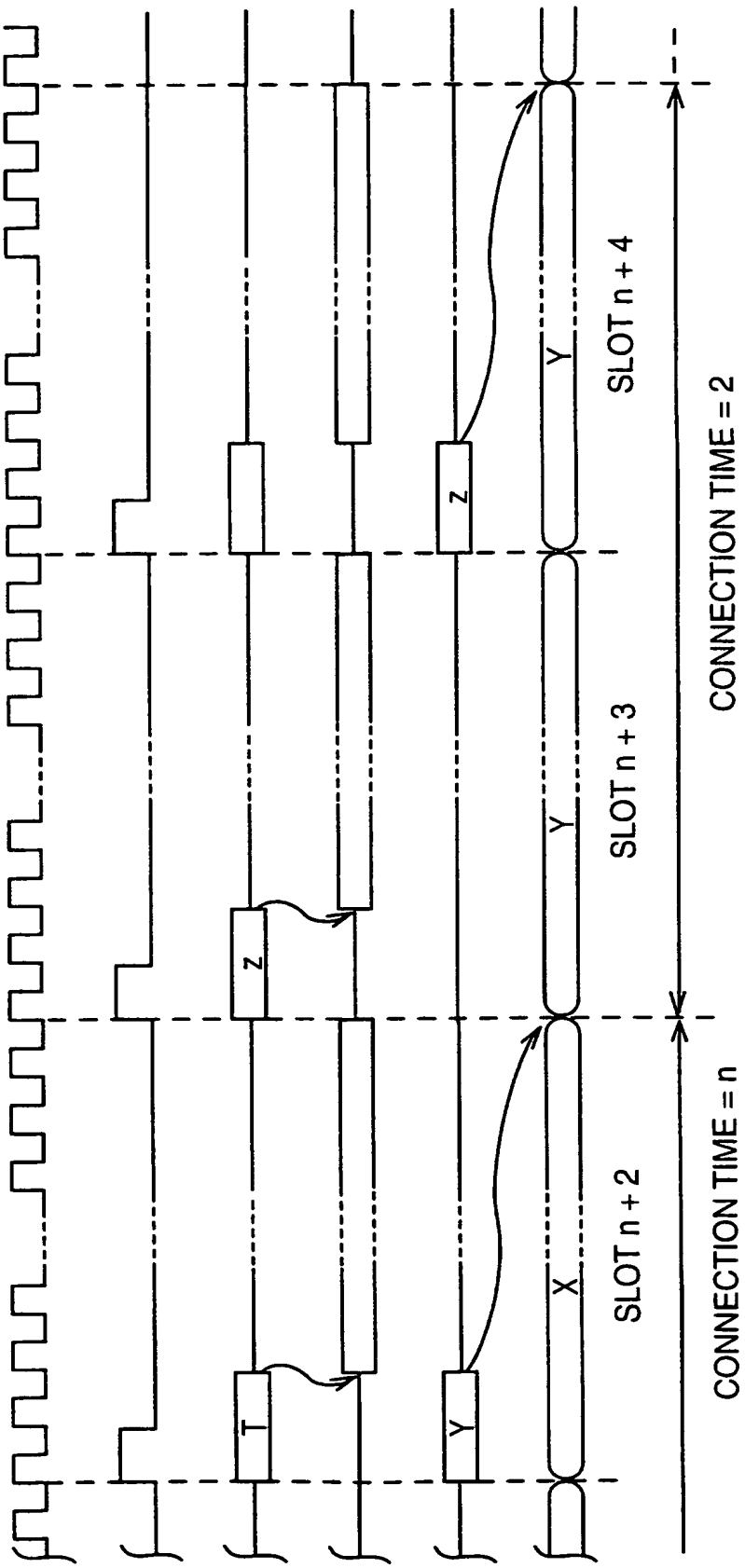
SLOT n + 4
SLOT n + 3
SLOT n + 2
CONNECTION TIME = 2
CONNECTION TIME = n
Z
Y
Z
Y
T
Y
X

FIG. 4B

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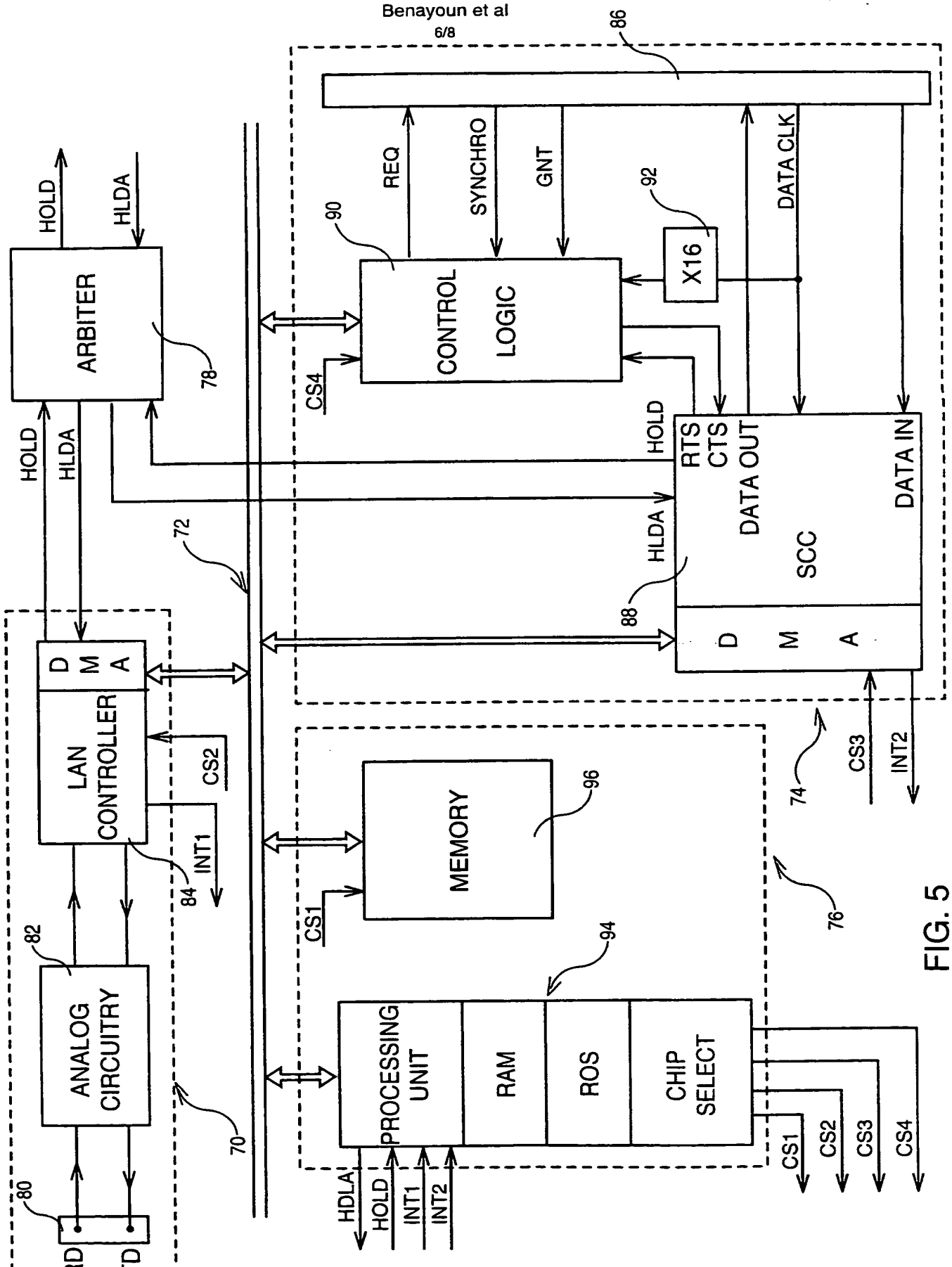

FIG. 5

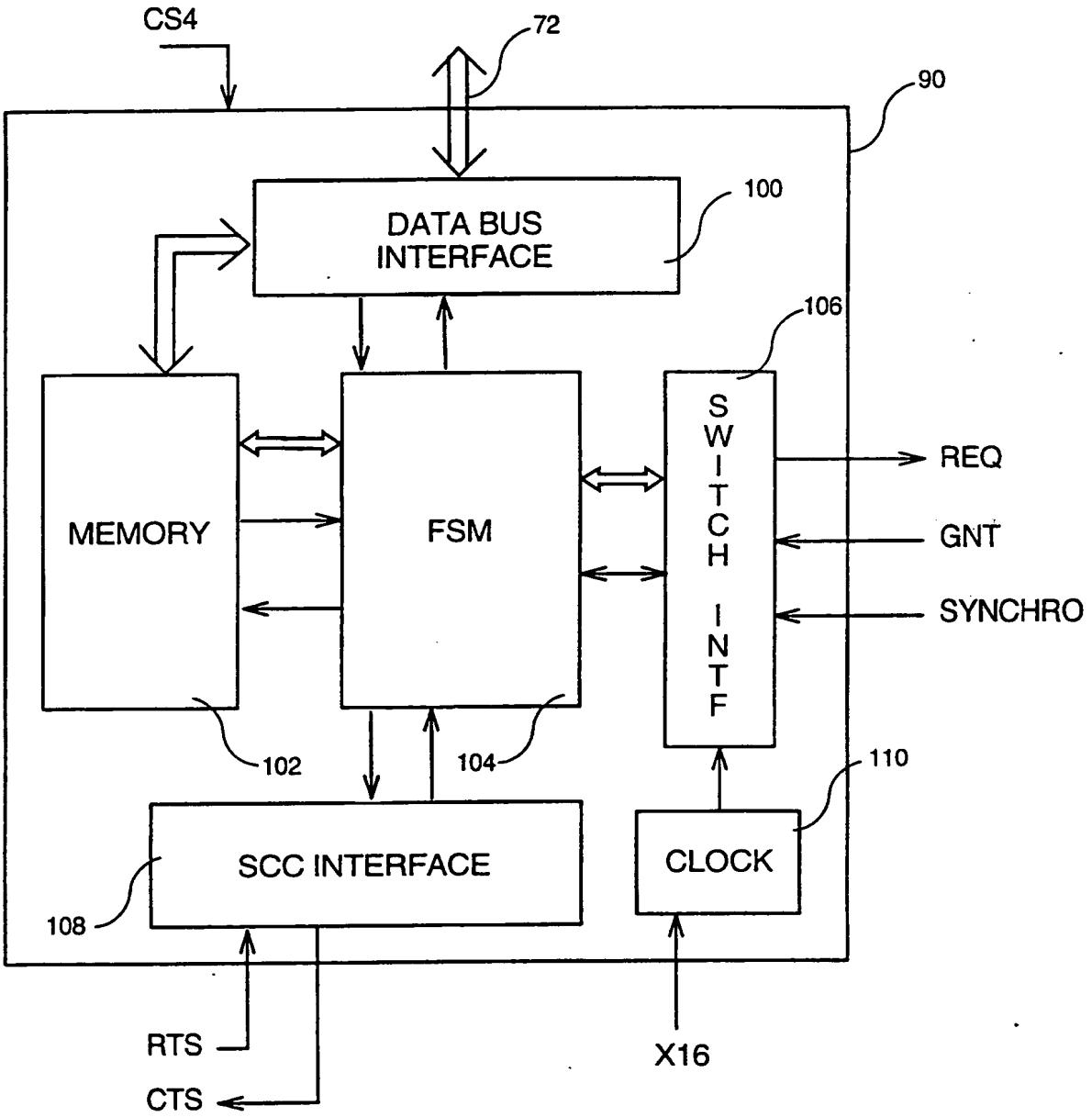
CS4
72
90
DATA BUS INTERFACE
100
106
MEMORY
FSM
SWITCH INTF
REQ
GNT
SYNCHRO
102
104
110
SCC INTERFACE
CLOCK
108
RTS
CTS
X16

FIG. 6

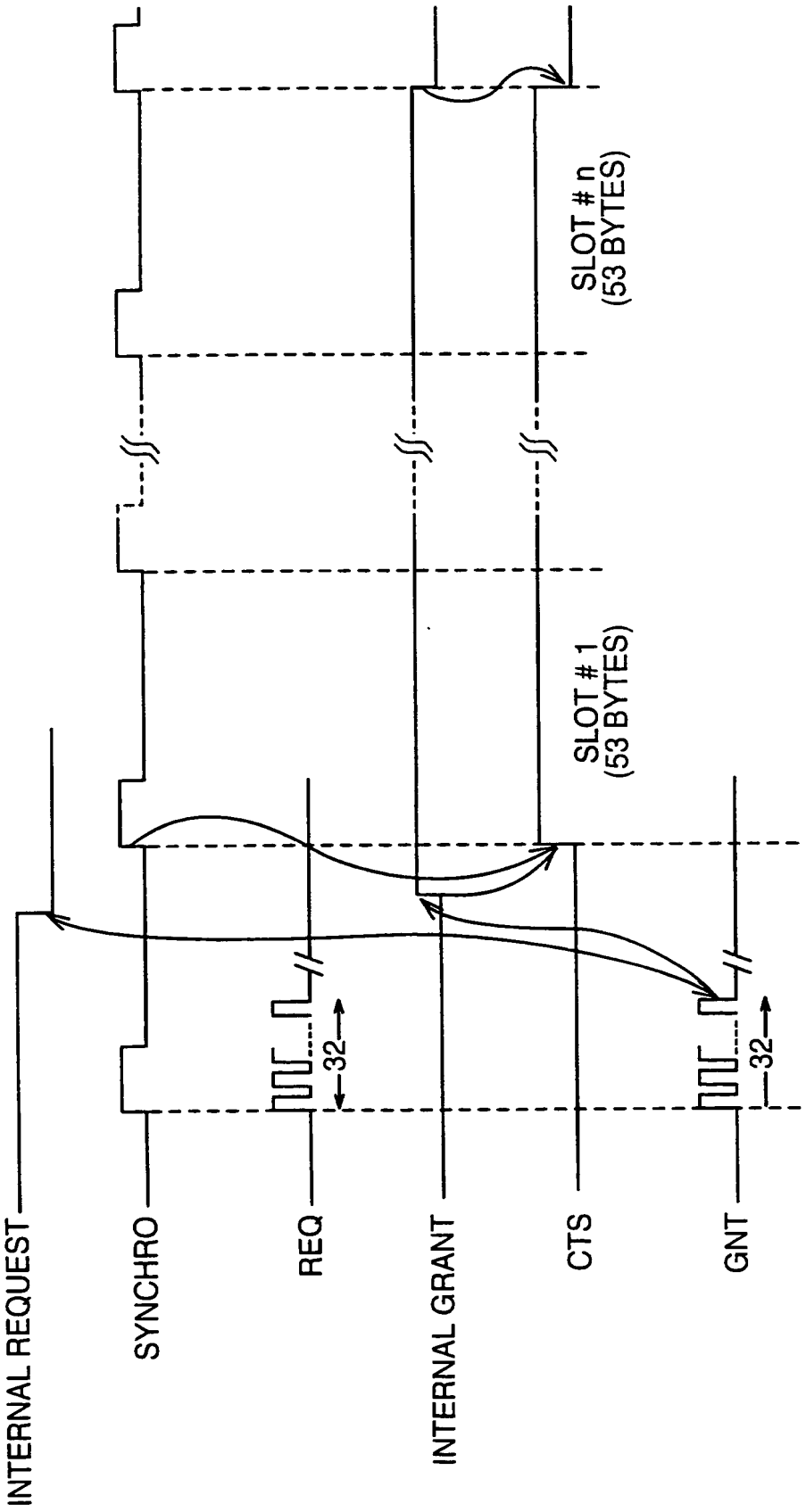
INTERNAL REQUEST
SYNCHRO
REQ
INTERNAL GRANT
CTS
GNT
32
32
SLOT # 1
(53 BYTES)
SLOT # n
(53 BYTES)

FIG. 7